

WHAT IS CLAIMED IS:

Sub B21
 1. A device for detecting a fixed pattern, said device being fed as a received signal with a pattern of a length of N chips, said received signal being obtained on dividing and re-arraying each of K symbols in terms of a chip period as a unit, K being a preset positive integer, each of said symbols being spread with a spread code at a rate of M chips per symbol, M being a preset positive integer, and on repeatedly inserting into the re-arrayed symbols a signature pattern of a length K having one chip period as a unit, by M times, where $N=K \times M$, said signature pattern being detected from said received signal,

said device comprising:

first-stage correlators taking correlation between M received signals spaced apart from one another by every K chips, and M spread code sequences obtained on jumping a spread code sequence of a length N by every K th chip to output correlation values associated with K signatures, respectively; and

a second-stage correlators taking correlation between the correlation values associated with K signatures output by said first-stage correlators and a pre-defined signature pattern.

2. The fixed pattern generator as defined in claim 1

wherein

said first-stage correlators are each fed with a spread code sequence of a length M obtained on decimating and re-arraying a spread code sequence of a length L generated by a

spread code generator at every K chips and classifying the re-
arrayed sequence into K to output correlation values associated
with K signatures.

3. The fixed pattern generator as defined in claim 2

wherein

said correlators make up K correlator blocks;

each of said K correlator blocks is made up of a plurality

5 of (R+1) correlators of a length M arranged in parallel with one
another;

in each of the correlator blocks, the first correlator of
said (R+1) correlators is fed with M received signals every K
chips and said spread code sequence to take correlation of a
length M, the second correlator is fed with M received signals,
10 at every K chips, having the received signal supplied to said
correlator as second data, as leading end data, and with a spread
code sequence which is said spread code sequence supplied to said
first correlator delayed by a delay element in synchronism with
an operating period, to take correlation with a length equal to
15 M, and so on, such that the (R+1)st correlator is fed with M
received signals at every K chips, having the received signal
supplied to said correlator as second data, as leading end data,
and with a spread code sequence which is said spread code
20 sequence supplied to said first correlator and delayed by R delay
elements in synchronism with an operating period, to take
correlation with a length equal to M.

4. The fixed pattern detection device as defined in claim 2 in which, in calculating correlation values shifted chip by chip for $N+L$ chips, where L , which is an integer divisible by K , denotes an indefinite time range where there exists said signature pattern;

wherein

each of said K correlator blocks has $L/K+1$ correlators of a length M , arranged in parallel.

5. The fixed pattern detection device as defined in claim 2 in which, in calculating correlation values shifted chip by chip for $N+L$ chips, where L , which is an integer divisible by K , denotes an indefinite time range during which there exists said signature pattern;

wherein

each of said K correlator blocks has $L/(n \times K) + 1$ correlators of a length M , arranged in parallel, where n is an integer not less than 2 provided that L is divisible by $n \times K$.

6. A device for detecting a fixed pattern, said device being fed as a received signal with a pattern of a length of N chips, said received signal being obtained on dividing and re-arraying each of a plurality of or K symbols in terms of a chip period as a unit, each said symbols being spread with a spread code at a rate of M chips per symbol, M being a preset positive integer, and on repeatedly inserting into the re-arrayed symbols a signature pattern of a length K having one chip period as a unit, by M times,

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said device comprising:

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(b) a spread code generator generating a spread code;

(c) a spread code re-arraying unit jumping and re-arraying the spread code generated by said spread code generator;

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(e) first-stage correlators comprised of K juxtaposed correlator blocks, each block being of an M chip length;

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(h) a correlation value storage memory storing the

(i) a correlation value storage memory controller controlling writing of the correlation value output from the first-stage correlators and reading-out of the correlation value from said received signal storage memory;

(j) a signature pattern storage unit storing and holding a preset signature pattern;

(k) second-stage correlators calculating correlation values between the correlation values read out from said correlation value storage memory controller and said signature pattern stored in said signature pattern storage unit; and

(1) a signature detector detecting the signature from the correlation value output from said second-stage correlators to output a fixed pattern detection signal.

7. The fixed pattern detection device as defined in claim 6 in which, in calculating correlation values shifted chip by chip for $N+L$ chips, where L , which is an integer divisible by K , denotes an indefinite time range during which there exists said signature pattern; said fixed pattern detection device having $L/K+1$ correlators arranged in a juxtaposed fashion, each with a length equal to M ,

wherein

said correlators are arrayed in blocks, and

in each of the correlator blocks, the first correlator of said $L/K+1$ correlators is fed with M received signals read out

from said received signal storage memory, at every K chips, and said spread code sequence, to take correlation of a length M;

the second correlator is fed with M received signals, at every K chips, having the received signal as supplied to said correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator delayed by a delay element in synchronism with an operating period, to take correlation with a length equal to M;

and so on;

such that the $L/K+1$ st correlator is fed with M received signals at every K chips, having the received signal as supplied to the L/K th correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator and delayed by L/K delay elements in synchronism with an operating period, to take correlation with a length equal to M.

8. The fixed pattern generator as defined in claim 6

wherein

each said K correlator blocks is made up of a plurality of $(R+1)$ correlators, each of a length M, arranged in parallel with one another;

in each of said correlator blocks, the first correlator of said $(R+1)$ correlators is fed with M received signals at every K chips and said spread code sequence as read out from said

the second correlator is fed with M received signals, at every K chips, having the received signal as supplied to said correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator from the spread code register and delayed by a

and so on;

such that the (R+1)st correlator is fed with M received signals at every K chips, having the received signal supplied to said Rth correlator as second data, as leading end data, and with a spread code sequence which is said spread code sequence supplied to said first correlator and delayed by R delay elements in synchronism with an operating period, to take correlation with a length equal to M.

wherein

each of said K correlator blocks has $L/(n \times K) + 1$ correlators arranged in parallel, where n is such an integer which is not less than 2 and which renders L divisible by $n \times K$.

10. The fixed pattern detection device as defined in claim 8 in which, in calculating correlation values shifted chip by chip for $N+L$ chips, where L , which is an integer divisible by K , denotes an L chip range that is an indefinite time range during

11. The fixed pattern detection device as defined in claim 6
wherein

12. The fixed pattern detection device as defined claim 6
wherein

13. A CDMA reception apparatus having the fixed pattern detection device as defined in any one of claim 1.

14. In a spread spectrum communication apparatus, a detection device for detecting a signature pattern from said received signal, said detection device being fed as an input a received signal with a pattern of a length of N chips, into which is repeatedly inserted M times a signature pattern of a length K with a one-chip period as a unit, said signature pattern, being obtained on dividing and re-arraying each signature of K symbols

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10 said device in the spread spectrum communication apparatus
comprising:

first-stage correlators taking correlation between M received signals spaced apart from one another at every K chips, and M spread code sequences obtained on decimating a spread code sequence of a length N at every K chips to output correlation values associated with K signatures; and

second-stage correlators taking correlation between the correlation values associated with K signatures output by said first-stage correlators and a pre-defined signature pattern.